

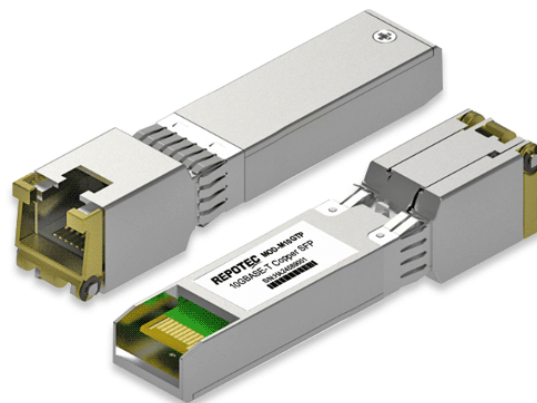
## MOD-M10GTP 10G-BASE-T Copper SFP+ Transceiver

### Features

- ✓ Supports Links up to 30m using Cat 6A Cable
- ✓ SFF-8431 and SFF-8432 MSA Compliant
- ✓ IEEE 802.3az and 802.3an Compliant
- ✓ IEEE 802.3bz for 5G&2.5G BASE-T
- ✓ Hot-pluggable SFP+ footprint
- ✓ TX Disable and RX Los function
- ✓ Fully metallic enclosure for Low EMI Emissions
- ✓ +3.3V single power supply
- ✓ Low Power Consumption (2.5W MAX @ 30m)
- ✓ Compact RJ-45 connector assembly
- ✓ Access to physical layer IC via 2-wire serial bus
- ✓ XFI/5GBASE-R/2500BASE-X/SGMII, SGMII Auto-Negotiation On
- ✓ Auto-negotiates with other 10GBase-T PHYs
- ✓ Supports 100/1000Base-T using Cat 5e cable or better
- ✓ MDI/MDIX Crossover
- ✓ Multiple Loopback Modes for Testing and Troubleshooting
- ✓ Built-in Cable Monitoring and Link Diagnostic
- ✓ Unshielded and Shielded cable support
- ✓ Operating case temperature range of 0°C to +70°C

### Applications

- ✓ 10 Gigabit Ethernet over Cat 6A/7 cable
- ✓ 5 Gigabit Ethernet over Cat 6A/7 cable
- ✓ 2.5 Gigabit Ethernet over Cat 6A/7 cable
- ✓ 1.25 Gigabit Ethernet over Cat 5e cable



## Description

RP-M10GTP Copper Small Form Pluggable Plus (SFP+) transceivers is high performance, cost effective module compliant with the 10 Gigabit Ethernet and 10G BASE-T standards as specified in IEEE 802.3-2015 and IEEE 802.3an, which supporting 10Gbps data-rate up to 30 meters reach over shielded twisted-pair category 6A cable. The module supports 10Gbps full duplex data-links with 16-level Pulse Amplitude Modulation (PAM) signals. The module provides standard serial ID information compliant with SFP+ MSA, which can be accessed with address of A0h via the 2wire serial bus. The physical IC can also be accessed via 2wire serial bus at address ACh.

## Pin Definitions

### Pin Diagram

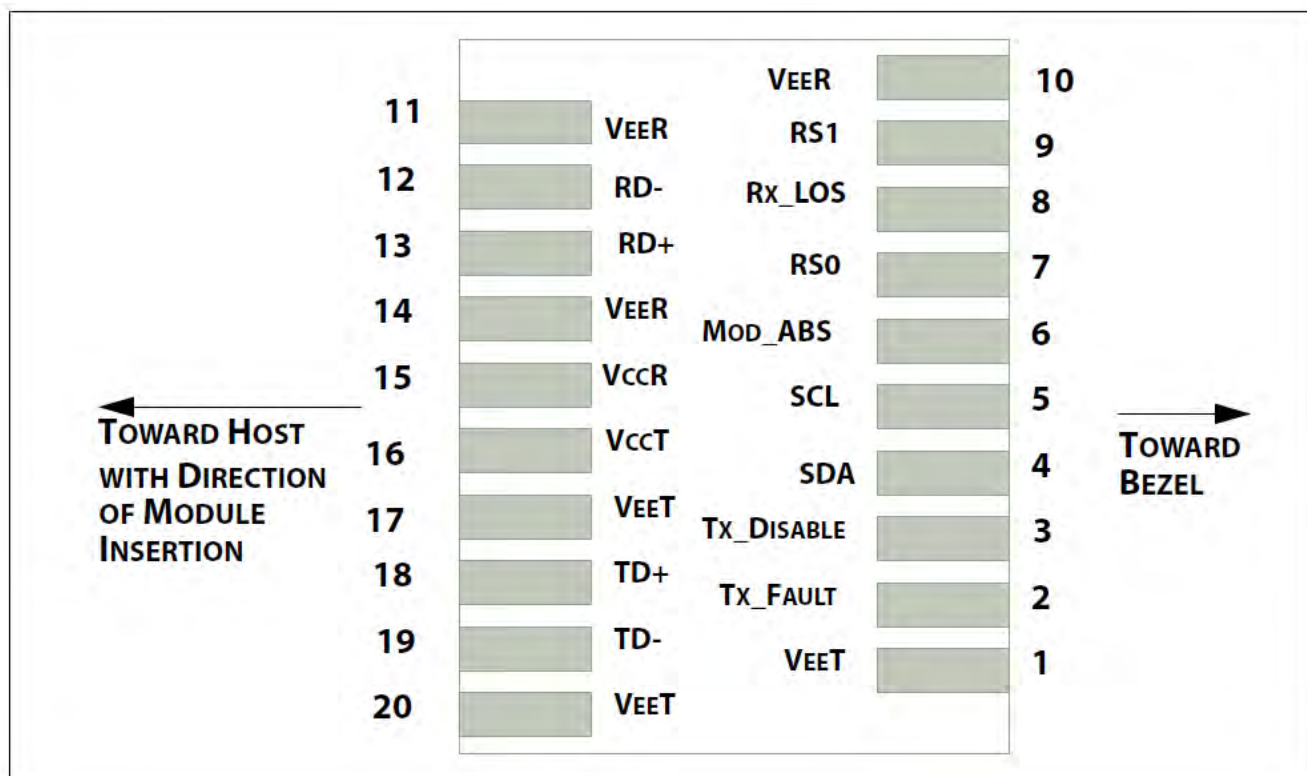


Figure 1. Pin Definitions

**Pin Descriptions**

Pin	Signal Name	Description	Notes
1	VeeT	Module Transmitter Ground	Note1
2	Tx_Fault	Module Transmitter Fault	Note2
3	Tx_Disable	Transmitter Disable; Turns off transmitter laser output	Note3
4	SDA	2-wire Serial Interface Data Line (Same as MOD-DEF2 in INF-8074i)	
5	SCL	2-wire Serial Interface Clock (Same as MOD-DEF1 in INF-8074i)	
6	Mod_ABS	Module Absent, connected to VeeT or VeeR in the module	
7	RS0	Rate Select 0, optionally controls SFP+ module receiver.	
8	Rx_LOS	Receiver Loss of Signal Indication (In FC designated as Rx_LOS and in Ethernet designated as Signal Detect)	Note2
9	RS1	Rate Select 1, optionally controls SFP+ module transmitter	
10	VeeR	Module Receiver Ground	Note1
11	VeeR	Module Receiver Ground	Note1
12	RD-	Receiver Inverted Data Output	
13	RD+	Receiver Non-Inverted Data Output	
14	VeeR	Module Receiver Ground	Note1
15	VccR	Module Receiver 3.3 V Supply	
16	VccT	Module Transmitter 3.3 V Supply	
17	VeeT	Module Transmitter Ground	Note1
18	TD+	Transmitter Non-Inverted Data Input	
19	TD-	Transmitter Inverted Data Input	
20	VeeT	Module Transmitter Ground	Note1

**Note:**

1. The module signal ground contacts, VeeR and VeeT, should be isolated from the module case.
2. This contact is an open collector/drain output contact and shall be pulled up on the host. Pull ups can be connected to one of several power supplies, however the host board.
3. Tx\_Disable is an input contact with a 4.7 k $\Omega$  to 10 k $\Omega$  pullup to VccT inside the module.

## +3.3V Volt Electrical Power Interface

+3.3V volt Electrical Power Interface						
Parameter	Symbol	Min	Typ	Max	Units	Notes/Conditions
Supply Current	Is		500	757	mA	2.5W max power over full range of voltage and temperature. See caution note below
Input Voltage	Vcc	3.13	3.3	3.47	V	Referenced to GND
Maximum Voltage	Vmax			3.6	V	

## Low-speed signals, electronic characteristics

Low-Speed Signals, Electronic Characteristics						
Parameter	Symbol	Min	Max	Units	Notes/Conditions	
SFP+ Output LOW	VOL	0	0.5	V	4.7k to 10k pull-up to host_Vcc, measured at host side of connector	
SFP+ Output HIGH	VOH	host_Vcc - 0.5	host_Vcc + 0.3	V	4.7k to 10k pull-up to host_Vcc, measured at host side of connector	
SFP+ Input LOW	VIL	0	0.8	V	4.7k to 10k pull-up to Vcc, measured at SFP side of connector	
SFP+ Input HIGH	VIH	2	Vcc + 0.3	V	4.7k to 10k pull-up to Vcc, measured at SFP side of connector	

## High-speed electrical interface, transmission line-SFP+

High-Speed Electrical Interface Transmission Line-SFP+						
Parameter	Symbol	Min	Typ	Max	Units	Notes/Conditions
Line Frequency	fL		800		MHz	16-level encoding, per IEEE 802.3
Tx Output Impedance	Zout,TX		100		Ohm	Differential, for all Frequencies between 1MHz and 800MHz
Rx Input Impedance	Zin,RX		100		Ohm	Differential, for all Frequencies between 1MHz and 800MHz

## High-speed electrical interface, host-SFP+

High-Speed Electrical Interface, Host-SFP						
Parameter	Symbol	Min	Typ	Max	Units	Notes/Conditions
Single ended data input swing	Vinsing	500	800	1100	mV	Differential
Single ended data output swing	Voutsing	500	800	1100	mV	Differential
Rise/Fall Time	Tr,Tf	25		47	psec	20%-80%



Tx Input Impedance	Zin		100		Ohm	Differential
Rx Output Impedance	Zout		100		Ohm	Differential

## General specifications

General						
Parameter	Symbol	Min	Typ	Max	Units	Notes/Conditions
Data Rate	BR	1		10	Gbps	IEEE 802.3 compatible. See Notes 2 through 4 below
Cable Length	L			30	m	Category 6A STP. BER <10-12

### Notes:

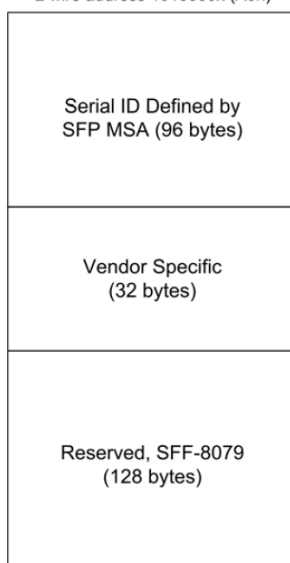
1. Clock tolerance is +/- 50 ppm
2. By default, the RP-M10GTP is a full duplex device in preferred master mode
3. Automatic crossover detection is enabled. External crossover cable is not required

## Environmental specifications

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		+70	°C
Storage Temperature		-40		+85	°C

## EEPROM Information

2 wire address 1010000x (A0h)



**Figure 2. 2-wire Serial Memory Map**

### Physical Layer IC Register

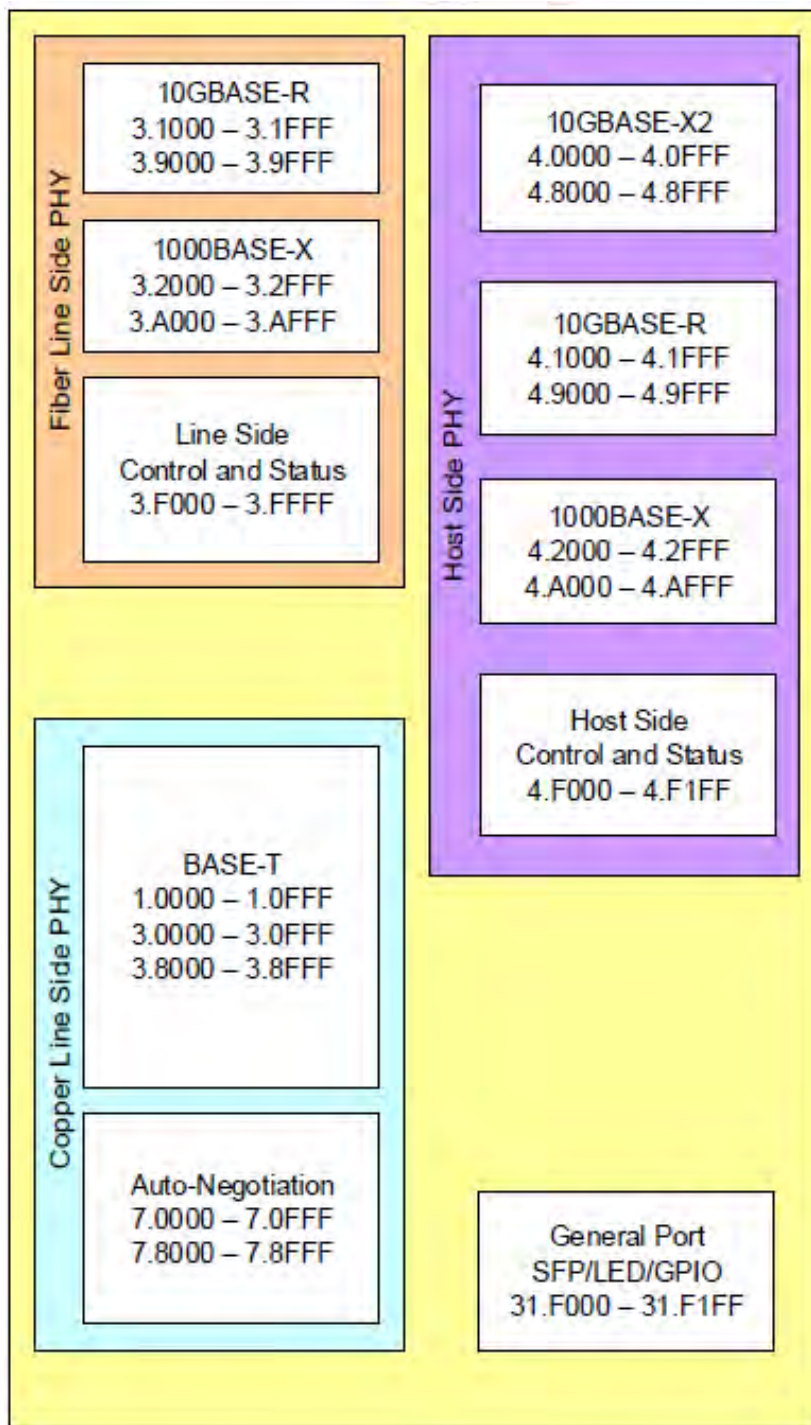


Figure 3. Phy IC Register List

### Recommended Host Board Power Supply Circuit

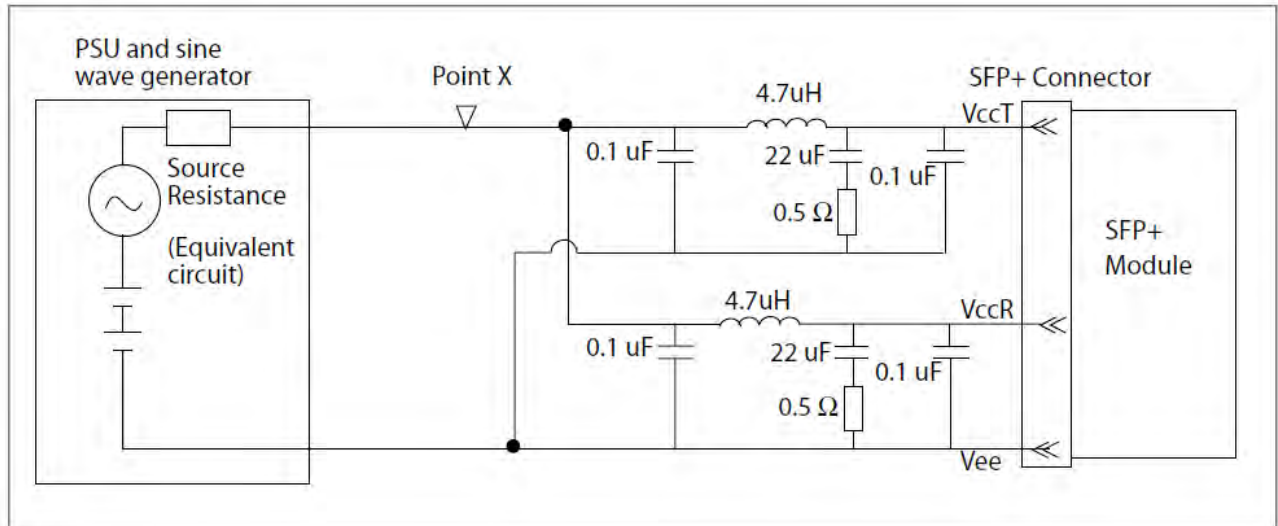


Figure 4. Recommended Host Board Power Supply Circuit

### Recommended Interface Circuit

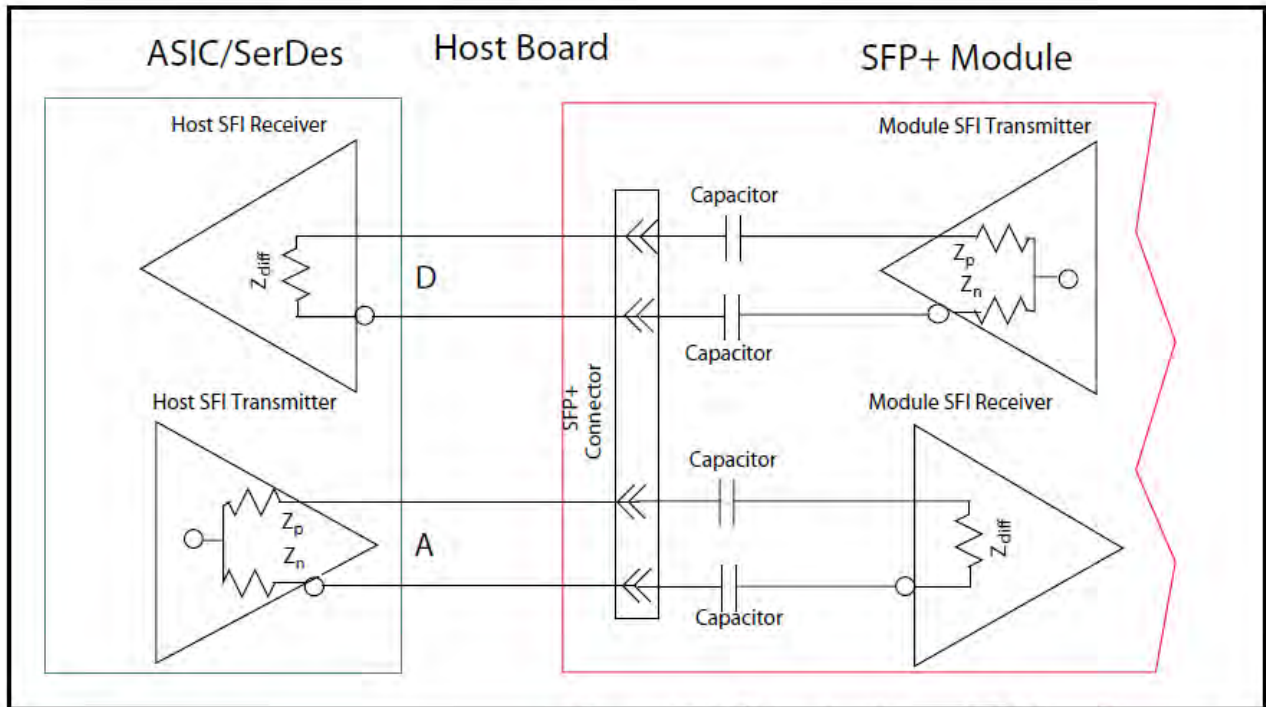
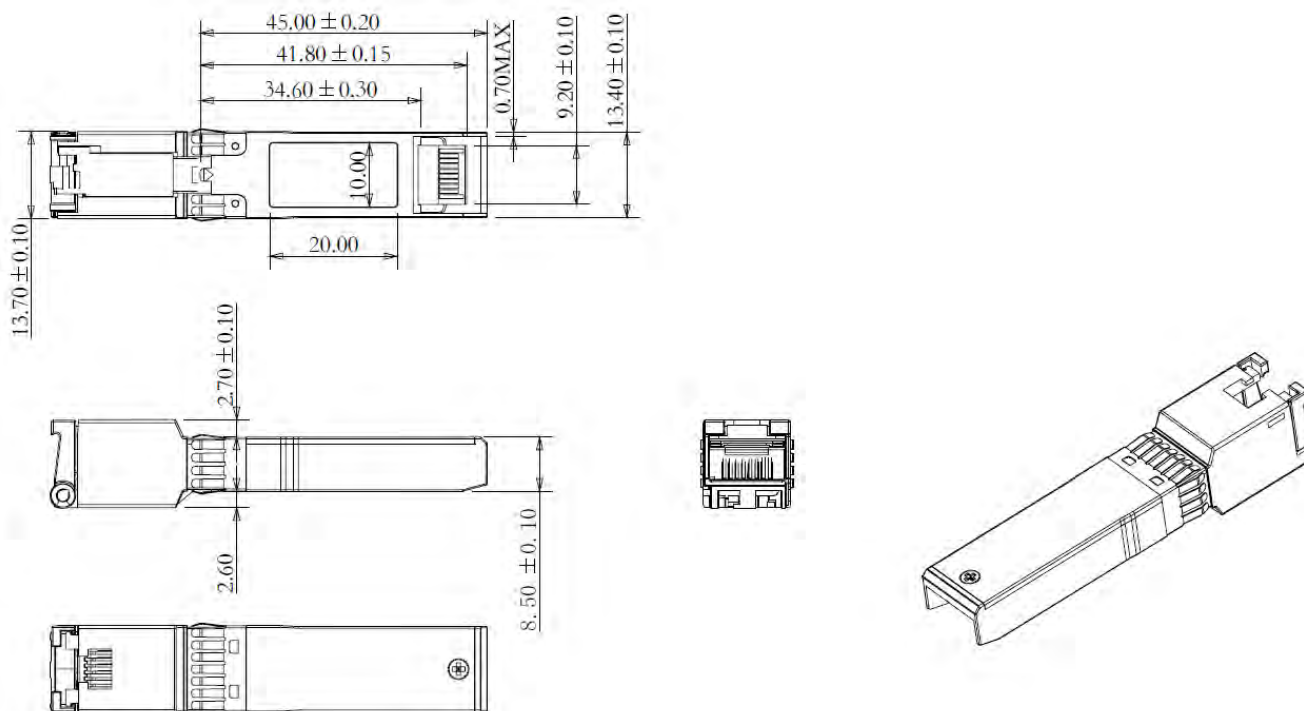


Figure 5. Recommended Host Board Power Supply Circuit



## Mechanical Specifications

The host-side of the MOD-M10GTP conforms to the mechanical specifications outlined in the SFP MSA1. The front portion of the SFP (part extending beyond the face plate of the host) is larger to accommodate the RJ-45 connector



**Figure 6. Mechanical dimensions**

## Regulatory Compliance

Feature	Standard
Environmental protection	2011/65/EU
CE EMC	EN55032 EN55035
FCC	47CFR FCC Part 15 Subpart B (Class B) ANSI C63.4:2014
RoHS	2011/65/EU



# RP-M10GTP Addendum

## 10GBASE-T SFP+ Register Access Application Note Version 1.0 10G

### BASE-T History

Number	Description	Date
1.0	Initial Publication of Document, Preliminary	February 1, 2018

#### Protocol for I2C to MDIO Bridge

The Transceiver contains a Bridge device to allow the Host I2C interface to communicate with the PHY's MDIO interface. In order for this to work the following protocol must be used.

I .The I2C Slave Address for the Bridge is 0x56 + R/W Bit or 0xAC for a write and 0xAD for a read.

II .To write to a PHY register the I2C Master needs to send a 6 Byte I2C frame.

1.The first Byte is the I2C Slave Address with R/W Bit = 0 or 0xAC.

2.The second Byte contains the 5 Bit MDIO Device Address in Bits 4:0 with Bits 7:5 = 0.

3.The next 2 Bytes are the 16 Bit Register Address with the MSB first, and the last 2 Bytes are the 16 Bit Data with the MSB first.

III.To read from a PHY register the I2C Master needs to first send a 4 Byte I2C frame.

1.The first Byte is the I2C Slave Address with R/W Bit = 0 or 0xAC.

2.The second Byte contains the 5 Bit MDIO Device Address in Bits 4:0 with Bit 5 = 1 and Bits 7:6 = 0.

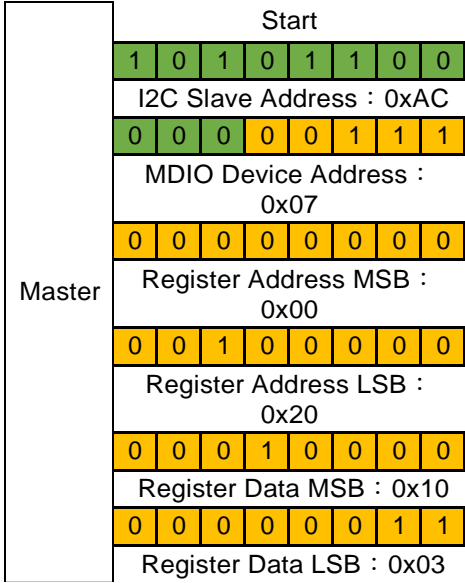
3.The next 2 Bytes are the 16 Bit Register Address with the MSB first.

4.Then the I2C Master starts a second frame by sending the I2C Slave Address with R/W Bit = 1 or 0xAD.

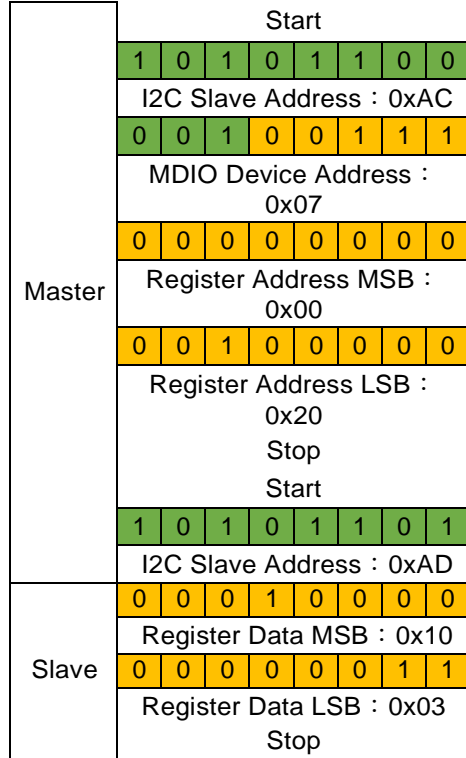
5.The I2C Master will then receive 2 Bytes containing the 16 Bit Data with the MSB first from the Slave.

**Examples:**

I . Write 0x1003 to Dev 07 Register 0x0020



II . Read 0x1003 from Dev 07 Register 0x0020



**Register Notations**

In the register description tables, the following notation in the R/W column is used to describe the read or write ability:

- R/W = Read or Write
- RO = Read Only
- LH = Latched High
- LL = Latched Low
- H = Fixed High
- L = Fixed Low
- SC = Self-clearing
- CR = Clear on Reset

Reserved Bits must be written as the default value and ignored when read.

### Special Cases and Applications

#### • **Using the 10GBASE-T SFP+ Module in a 1G switch and linked to a 1000Base-T port on Media side**

In this case, no configuration is needed for the module. Simply making the module link on the network side first and then link on the system side, the module will auto-negotiate the rate to

1000Mbps.

#### • **Set the 10GBASE-T SFP+ Module in 10G ONLY mode**

To set the 10GBASE-T SFP+ module in 10G only mode on Media side, the following configuration instructions need to be written to the module before the cable plugged in:

Write 0x1001 to Dev 07 Register 0x0010 Write  
0x0010 to Dev 07 Register 0x8000

### Cable Monitoring

#### 1. **Start Test (1.C00D.15)**

Setting bit to “1” starts a single execution of the TDR test. Upon initiation, the bit is set to “0” by the internal controller, allow up to 1ms. The Test Status bit indicates whether the test is still running. This function depends on the setting of the Break Link bit.

#### 2. **Break Link (1.C00D.12)**

Setting bit to “1” will cause the link to drop and retest the cable when the Start Test bit is set. Upon initiation of Start Test, this bit is set to “0” by the internal controller, allow up to 1ms. The Test Status bit indicates whether the test is still running.

#### 3. **Cable Diagnostic Results 1 (1.C00E)**

Results of the TDR test are reported for channels D, C, B and A in bits 15:12, 11:8, 7:4 and 3:0 respectively. The 4-bit termination codes for each channel are:

0xf - 0x5: reserved  
0x4: inter-pair short  
0x3: intra-pair short  
0x2: pair open

0x1: pair ok, no fault

0x0: invalid or incomplete test

#### 4. **Cable Diagnostic Results 2 & 3 (1.C00F to 1.C010)**

The cable length or distance to fault is reported in meters for channels D, C, B and A in register bits 1.C00F.15:8, 1.C00F.7:0, 1.C010.15:8, 1.C010.7:0 respectively.

## Diagnostics

### • Reading the Temperature of the PHY

1. Write 0x4D00 to Dev 31 Register 0xF08A.
2. Wait 8~10 second.
3. Read the Value from Dev 31 Register 0xF08A until the reading is 0x4Dxx (≠0x4D00).
4. PHY temperature(Celsius)= 31.F08A.7:0 - 75.
5. Read the Value from Dev 31 Register 0xF08A is 0x4D79,then PHY temperature(Celsius) =0x79-75=120-75=45°C;

### • Linking status on Media side

Bit 10 of Dev 3 Register 0x8008 indicate the linking rate of the Media side. 1 = Link is up on Media side

0 = Link is down on Media side

### • Linking rate on Media side

Bit 15:14 of Dev 3 Register 0x8008 indicate the linking rate of the Media side. 11 = 10GBASE-T

10 = 1000 Mbps

01 = 100 Mbps

00 = 10 Mbps

### Loopback Mode

The 10GBASE-T SFP+ supports loopback modes on both MAC side and Line side.

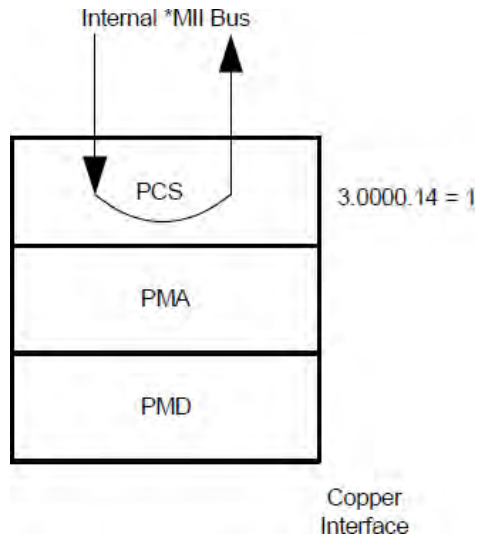
### • MAC Side loopback

10GBASE-T SFP+ in MAC loopback mode sends packets transmitted to it back to the switch / MAC. The incoming packet must be Ethernet-Compliant.

### • MAC loopback at PCS of 10GBase-T



Set Bit 14 of Dev 3 Register 0x0000 to 1



- **Line Side loopback**

10GBASE-T SFP+ in Line loopback mode loops the data from the receive path back to the transmit path on the copper interface. The incoming packet must be Ethernet-Compliant.

- **Line loopback at PCS for 10G/5G/2.5G mode.**

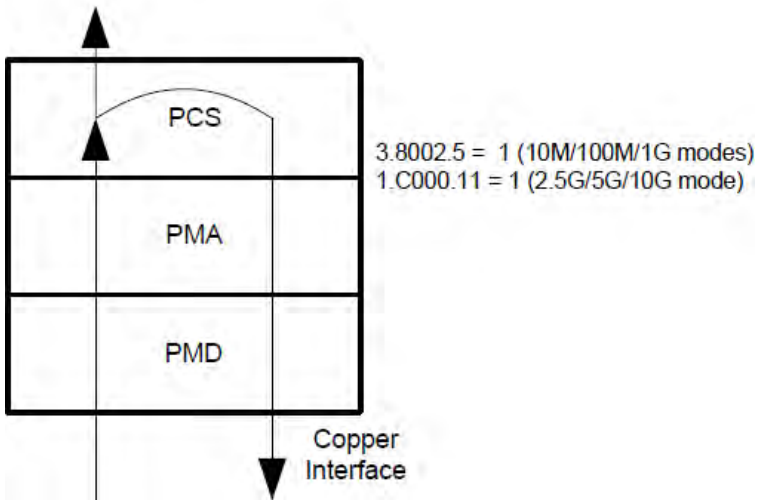
Set Bit 11 of Dev 1 Register 0xC000 to 1

- **Line loopback at PCS for 1000M/100M/10M mode.**

Set Bit 5 of Dev 3 Register 0x8002 to 1

- **Line loopback for HOST.**

Set Bit 12 of Dev 4 Register 0xF003 to 1  
Internal \*MII Bus



**PMA/PMD registers**

Register address	Register name	Subclause
1.0	PMA/PMD control 1 register	45.2.1.1
1.1	PMA/PMD status 1 register	45.2.1.2
1.2, 1.3	PMA/PMD device identifier	45.2.1.3
1.4	PMA/PMD speed ability	45.2.1.4
1.5, 1.6	PMA/PMD devices in package	45.2.1.5
1.7	PMA/PMD control 2 register	45.2.1.6
1.8	PMA/PMD status 2 register	45.2.1.7
1.9	PMA/PMD transmit disable register	45.2.1.8
1.11	PMA/PMD extended ability register	45.2.1.10
1.12	10G-EPON PMA/PMD ability register	45.2.1.11
1.14, 1.15	PMA/PMD package identifier	45.2.1.13
1.129	10GBASE-T status	45.2.1.59
1.130	10GBASE-T pair swap and polarity	45.2.1.60
1.131	10GBASE-T TX power backoff and PHY short	45.2.1.61
1.132	10GBASE-T test mode	45.2.1.62
1.133	10GBASE-T SNR operating margin channel A	45.2.1.66
1.134	10GBASE-T SNR operating margin channel B	45.2.1.67
1.135	10GBASE-T SNR operating margin channel C	45.2.1.68
1.136	10GBASE-T SNR operating margin channel D	45.2.1.69
1.137	10GBASE-T minimum margin channel A	45.2.1.70
1.138	10GBASE-T minimum margin channel B	45.2.1.71
1.139	10GBASE-T minimum margin channel C	45.2.1.72
1.140	10GBASE-T minimum margin channel D	45.2.1.73
1.141	10GBASE-T RX signal power channel A	45.2.1.74
1.142	10GBASE-T RX signal power channel B	45.2.1.75
1.143	10GBASE-T RX signal power channel C	45.2.1.76
1.144	10GBASE-T RX signal power channel D	45.2.1.77
1.145 through 1.146	10GBASE-T skew delay	45.2.1.78
1.147	10GBASE-T fast retrain status and control register	45.2.1.79

Table 1—PMA/PMD Control 1 Register (Device 1, Register 0x0000)

Bit(s)	Name	Description	R/W	Default
15	Software Reset	This register will soft reset the copper unit. 1 = Reset 0 = Normal	R/W, SC	0
14	Reserved	Set to 0	R/W	0
13	Speed Select	A change in this bit while 7.0000.12 is 0 will cause Auto-Negotiation to restart. bit 6, bit 13 00 = 10Mbps 01 = 100Mbps 10 = 1000 Mbps (also sets 7.0.12 to 1) 11 = Bits 5:2 Determine Speed (also sets 7.0.13:12 to 11b)	R/W	1
12	Reserved	Set to 0	R/W	0
11	Low Power	This register will power down the copper unit. 1 = Low Power mode 0 = Normal	R/W	0
10:7	Reserved	Set to 0	R/W	0
6	Speed Select	A change in this bit while 7.0000.12 is 0 will cause Auto-Negotiation to restart. bit 6, bit 13 00 = 10Mbps 01 = 100Mbps 10 = 1000 Mbps (also sets 7.0.12 to 1) 11 = Bits 5:2 determine speed (also sets 7.0.13:12 to 11b)	R/W	1
5:2	Speed Select	A change in this bit while 7.0000.12 is 0 will cause Auto-Negotiation to restart. 0000 = 10 Gbps 0110 = 2.5 Gbps 0111 = 5 Gbps These bits only valid if bits 13/6 are 11b	R/W	0
1	Reserved	Set to 0	R/W	0
0	PMA Loopback	1 = Drop link and loop data back in 10GBASE-T PMA toward MAC 0 = Normal operation	R/W	0



Table 2—PMA/PMD Status 1 Register (Device 1, Register 0x0001)

Bit(s)	Name	Description	R/W	Default
15:8	Reserved	This register will soft reset the copper unit. 1 = Reset 0 = Normal	RO	0
7	Fault	Set to 0	RO	0
6:3	Reserved	A change in this bit while 7.0000.12 is 0 will cause Auto-Negotiation to restart. bit 6, bit 13 00 = 10Mbps 01 = 100Mbps 10 = 1000 Mbps (also sets 7.0.12 to 1) 11 = Bits 5:2 Determine Speed (also sets 7.0.13:12 to 11b)	RO	0
2	Link Status	Set to 0	RO, LL	0
1	Low Power Ability	This register will power down the copper unit. 1 = Low Power mode 0 = Normal	RO	1
0	Reserved	Set to 0	RO	0

Table 3—PMA/PMD Device Identifier 1 Register (Device 1, Register 0x0002)

Bit(s)	Name	Description	R/W	Default
15:0	Organizationally Unique Identifier Bit 3:18	Set to 0000000000101011	RO	0x2B

Table 4—PMA/PMD Device Identifier 2 Register (Device 1, Register 0x0003)

Bit(s)	Name	Description	R/W	Default
15:10	Organizationally Unique Identifier Bit 19:24	Set to 000010	RO	000010
9:4	Model Number	Set to 011010	RO	011010
3:0	Revision Number	Rev Number	RO	1011

Table 5—PMA/PMD Speed Ability Register (Device 1, Register 0x0004)

Bit(s)	Name	Description	R/W	Default
15	Reserved	Set to 000000000	RO	0
14	5G Capable	1 = PMA/PMD is capable of operating at 5 Gbps	RO	0
13	2.5G Capable	1 = PMA/PMD is capable of operating at 2.5 Gbps	RO	0
12:7	Reserved	Set to 000000000	RO	0
6	10M Capable	1 = PMA/PMD is capable of operating at 10 Mbps	RO	1
5	100M Capable	1 = PMA/PMD is capable of operating at 100 Mbps	RO	1
4	1000M Capable	1 = PMA/PMD is capable of operating at 1000 Mbps	RO	1
3:1	Reserved	Set to 000	RO	0
0	10G Capable	1 = PMA/PMD is capable of operating at 10 Gbps	RO	1

Table 6—PMA/PMD Devices In Package 1 Register (Device 1, Register 0x0005)

Bit(s)	Name	Description	R/W	Default
15:8	Reserved	Set to 00000000	RO	0
7	Auto-Negotiation	1 = Auto-negotiation present in package	RO	1
6	Present	Set to 0	RO	0
5	Reserved	1 = DTE XS present in package 0 = DTE XS not present in package	RO	0
4	DTE XS Present	1 = PHY XS present in package 0 = PHY XS not present in package	RO	1
3	PHY XS Present	1 = PCS present in package 0 = PCS not present in package	RO	1
2	PCS Present	1 = WIS present in package 0 = WIS not present in package	RO	0
1	PMD/PMA Present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO	1
0	Clause 22 Registers Present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO	0

Table 7—PMA/PMD Devices In Package 2 Register (Device 1, Register 0x0006)

Bit(s)	Name	Description	R/W	Default
15	Vendor Specific Device 2 Present	1 = Vendor specific device 2 present 0 = Vendor specific device 2 not present	RO	1
14	Vendor Specific Device 1 Present	1 = Vendor specific device 1 present 0 = Vendor specific device 1 not present	RO	1
13:0	Reserved	Set to 00000000000000	RO	0

Table 8—PMA/PMD control 2 Register (Device 1, Register 0x0007)

Bit(s)	Name	Description	R/W	Default
15:6	Reserved	Set to 000000000000.	R/W	0
5:0	PMA/PMD Type	Please refer to IEEE 45.2.1.6 for details 001001 = 10GBASE-T 110001 = 5GBASE-T 110000 = 2.5GBASE-T This register is ignored by the PHY. Actual PMA/PMD used is determined by auto-negotiations, or PHY mode select.	R/W	001001

Table 9—PMA/PMD Status 2 Register (Device 1, Register 0x0008)

Bit(s)	Name	Description	R/W	Default
15:14	Device Present	10 = Device responding to this address	RO	10
13	Transmit Fault Ability	1 = PMA/PMD has ability to detect a fault condition on the transmit path 0 = PMA/PMD does not have ability to detect a fault condition on the transmit path	RO	0
12	Receive Fault Ability	1 = PMA/PMD has ability to detect a fault condition on the receive path 0 = PMA/PMD does not have ability to detect a fault condition on the receive path	RO	1
11	Transmit Fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO, LH	0
10	Receive Fault	1 = Fault condition on receive path 0 = No fault condition on receive path	RO, LH	1
9	Extended Abilities	1 = PMA/PMD Extended abilities listed in 1.11 0 = No extended abilities listed in 1.11	RO	1
8	PMD Transmit Disable Ability	1 = PMD has the ability to disable the transmit path 0 = PMD does not have the ability to disable the transmit path	RO	1

7	10GBASE-SR Ability	1 = Able 0 = Not able	RO	0
6	10GBASE-LR Ability	1 = Able 0 = Not able	RO	0
5	10GBASE-ER Ability	1 = Able 0 = Not able	RO	0
4	10GBASE-LX4 Ability	1 = Able 0 = Not able	RO	0
3	10GBASE-SW Ability	1 = Able 0 = Not able	RO	0
2	10GBASE-LW Ability	1 = Able 0 = Not able	RO	0
1	10GBASE-EW Ability	1 = Able 0 = Not able	RO	0
0	PMA Loopback Ability	1 = Able 0 = Not able	RO	1

Table 10—PMA Transmit Disable Register (Device 1, Register 0x0009)

Bit(s)	Name	Description	R/W	Default
15:	Reserved	Set to 000000000000	R/W	0
4	PMA transmit disable Pair D	0 = Enable transmitter 1 = Disable transmitter	RO	0
3	PMA transmit disable Pair C	0 = Enable transmitter 1 = Disable transmitter	RO	0
2	PMA transmit disable Pair B	0 = Enable transmitter 1 = Disable transmitter	RO	0
1	PMA transmit disable Pair A	0 = Enable transmitter 1 = Disable transmitter	RO	0
0	Global PMA transmit disable (all pairs)	0 = Enable transmitter 1 = Disable transmitter	RO	0



Table 11—PMA/PMD Extended Ability Register (Device 1, Register 0x000B)

Bit(s)	Name	Description	R/W	Default
15	Reserved	Set to 0	RO	0
14	2.5/5GBASE-T	1 = PMA/PMD has 2.5G/5G Extended Abilities in 1.21	RO	0
13:9	Reserved	Set to 00000	RO	0
8	10BASE-T	1 = PMA/PMD is able to perform 10BASE-T	RO	1
7	100BASE-TX	1 = PMA/PMD is able to perform 100BASE-TX	RO	1
6	1000BASE-KX	0 = PMA/PMD is not able to perform 1000BASE-KX	RO	0
5	1000BASE-T	1 = PMA/PMD is able to perform 1000BASE-T	RO	1
4	10GBASE-KR	0 = PMA/PMD is not able to perform 10GBASE-KR	RO	0
3	10GBASE-KX4	0 = PMA/PMD is not able to perform 10GBASE-KX4	RO	0
2	10GBASE-T	1 = PMA/PMD is able to perform 10GBASE-T	RO	1
1	10GBASE-LRM	0 = PMA/PMD is not able to perform 10GBASE-LRM	RO	0
0	10GBASE-CX4	0 = PMA/PMD is not able to perform 10GBASE-CX4	RO	0

Table 12—PMA/PMD Package Identifier 1 Register (Device 1, Register 0x000E)

Bit(s)	Name	Description	R/W	Default
15:0	Organizationally Unique Identifier Bit 3:18	Set to 0000000000101011	RO	0x2B

Table 13—PMA/PMD Package Identifier 2 Register (Device 1, Register 0x000F)

Bit(s)	Name	Description	R/W	Default
15:10	Organizationally Unique Identifier Bit 19:24	Set to 000010	RO	000010
9:4	Model Number	Same as 1.0003.9:4	RO	011010
3:0	Revision Number	Same as 1.0003.3:0	RO	1011

Table 14—Status Register Valid Register (Device 1, Register 0x0081)

Bit(s)	Name	Description	R/W	Default
15:1	Reserved	Set to 0000000000000000	RO	0
0	LP Information Valid	1 = Link Partner Information is Valid 0 = Link Partner Information is Not Valid	RO	0

Table 15—10G Pair Swap and Polarity Register (Device 1, Register 0x0082)

Bit(s)	Name	Description	R/W	Default
15:12	Reserved	Set to 0000	RO	0000
11	Pair D Polarity	1 = Polarity of Pair D is Reversed 0 = Polarity of Pair D is Not Reversed If register 1.0082.1 = 1 then this bit reflects the condition on MDIP/N[2], otherwise this bit reflects the condition on MDIP/N[3]. This bit should be ignored in 10/100BASE-T.	RO	0
10	Pair C Polarity	1 = Polarity of Pair C is Reversed 0 = Polarity of Pair C is Not Reversed If register 1.0082.1 = 1 then this bit reflects the condition on MDIP/N[3], otherwise this bit reflects the condition on MDIP/N[2]. This bit should be ignored in 10/100BASE-T.	RO	0
9	Pair B Polarity	1 = Polarity of Pair B is Reversed 0 = Polarity of Pair B is Not Reversed If register 1.0082.0 = 1 then this bit reflects the condition on MDIP/N[0], otherwise this bit reflects the condition on MDIP/N[1]. This bit should be ignored in 10/100BASE-T.	RO	0
8	Pair A Polarity	1 = Polarity of Pair A is Reversed 0 = Polarity of Pair A is Not Reversed If register 1.0082.0 = 1 then this bit reflects the condition on MDIP/N[1], otherwise this bit reflects the condition on MDIP/N[0]. This bit should be ignored in 10/100BASE-T.	RO	0
7:2	Reserved	Set to 000000	RO	0
1:0	MDI/MDIX Connection	00 = Pair A/B Crossover and Pair C/D Crossover 01 = Pair C/D Crossover Only 10 = Pair A/B Crossover Only 11 = No Crossover The no crossover case is where the receiver sees MDIP/N[0] = Pair B MDIP/N[1] = Pair A MDIP/N[2] = Pair D MDIP/N[3] = Pair C	RO	11

Table 16—10GBASE-T TX Power Level Setting Register (Device 1, Register 0x0083)

Bit(s)	Name	Description	R/W	Default
15:13	Link Partner TX Power Level Setting	1.0083.15:13 is valid only if 1.0081.0 is set to 1. 000 = 0 dB 001 = 2 dB 010 = 4 dB 011 = 6 dB 100 = 8 dB 101 = 10 dB 110 = 12 dB 111 = 14 Db	RO	000
12:10	TX Power Level Setting	000 = 0 dB 001 = 2 dB 010 = 4 dB 011 = 6 dB 100 = 8 dB 101 = 10 dB 110 = 12 dB 111 = 14 dB	RO	000
9:1	Reserved	Set to 000000000	RO	0
0	Short Reach Mode	1 = PHY is operating in short reach mode 0 = PHY is not operating in short reach mode	R/W	0

Table 17—10GBASE-T Test Mode Register (Device 1, Register 0x0084)

Bit(s)	Name	Description	R/W	Default
15:13	Test Mode Control	000 = Normal Operation 001 = Test Mode 1 010 = Test Mode 2 011 = Test Mode 3 100 = Test Mode 4 101 = Test Mode 5 110 = Test Mode 6 111 = Test Mode 7 Note: For Test Mode and Tone tests, use register 1.0000 to set the line speed.	R/W	000
12:10	Transmitter Test Frequencies	000 = Reserved 001 = Dual Tone 1 010 = Dual Tone 2 011 = Reserved 100 = Dual Tone 3 101 = Dual Tone 4 110 = Dual Tone 5 111 = Reserved Note: For Test Mode and Tone tests, use register 1.0000 to set the line speed.	R/W	000
9:0	Reserved	Set to 0000000000	R/W	0

Table 18—10GBASE-T SNR Operating Margin Channel A Register (Device 1, Register 0x0085)

Bit(s)	Name	Description	R/W	Default
15:0	SNR Operating Margin Channel A	0x7F81 = -12.7 dB 0x8000 = 0 dB 0x807F = 12.7 dB Each bit represents 0.1dB	RO	0

Table 19—10GBASE-T SNR Operating Margin Channel B Register (Device 1, Register 0x0086)

Bit(s)	Name	Description	R/W	Default
15:0	SNR Operating Margin Channel B	0x7F81 = -12.7 dB 0x8000 = 0 dB 0x807F = 12.7 dB Each bit represents 0.1dB	RO	0



Table 20—10GBASE-T SNR Operating Margin Channel C Register (Device 1, Register 0x0087)

Bit(s)	Name	Description	R/W	Default
15:0	SNR Operating Margin Channel C	0x7F81 = -12.7 dB 0x8000 = 0 dB 0x807F = 12.7 dB Each bit represents 0.1dB	RO	0

Table 21—10GBASE-T SNR Operating Margin Channel D Register (Device 1, Register 0x0088)

Bit(s)	Name	Description	R/W	Default
15:0	SNR Operating Margin Channel D	0x7F81 = -12.7 dB 0x8000 = 0 dB 0x807F = 12.7 dB Each bit represents 0.1dB	RO	0

Table 22—10GBASE-T Minimum Margin Channel A Register (Device 1, Register 0x0089)

Bit(s)	Name	Description	R/W	Default
15:0	Minimum Margin Channel A	0x7F81 = -12.7 dB 0x8000 = 0 dB 0x807F = 12.7 dB Each bit represents 0.1dB	RO, RS	0xFFFF

Table 23—10GBASE-T Minimum Margin Channel B Register (Device 1, Register 0x008A)

Bit(s)	Name	Description	R/W	Default
15:0	Minimum Margin Channel B	0x7F81 = -12.7 dB 0x8000 = 0 dB 0x807F = 12.7 dB Each bit represents 0.1dB	RO, RS	0xFFFF

Table 24—10GBASE-T Minimum Margin Channel C Register (Device 1, Register 0x008B)

Bit(s)	Name	Description	R/W	Default
15:0	Minimum Margin Channel C	0x7F81 = -12.7 dB 0x8000 = 0 dB 0x807F = 12.7 dB Each bit represents 0.1dB	RO, RS	0xFFFF

Table 25—10GBASE-T Minimum Margin Channel D Register (Device 1, Register 0x008C)

Bit(s)	Name	Description	R/W	Default
15:0	Minimum Margin Channel D	0x7F81 = -12.7 dB 0x8000 = 0 dB 0x807F = 12.7 dB Each bit represents 0.1dB	RO, RS	0xFFFF

Table 26—10GBASE-T RX Signal Power Channel A Register (Device 1, Register 0x008D)

Bit(s)	Name	Description	R/W	Default
15:0	RX Signal Power Channel A	0x7F38 = -20.0 dBm 0x8000 = 0 dBm 0x8037 = 5.5 dBm Each bit represents 0.1 dBm	RO	0

Table 27—10GBASE-T RX Signal Power Channel B Register (Device 1, Register 0x008E)

Bit(s)	Name	Description	R/W	Default
15:0	RX Signal Power Channel B	0x7F38 = -20.0 dBm 0x8000 = 0 dBm 0x8037 = 5.5 dBm Each bit represents 0.1 dBm	RO	0

Table 28—10GBASE-T RX Signal Power Channel C Register (Device 1, Register 0x008F)

Bit(s)	Name	Description	R/W	Default
15:0	RX Signal Power Channel C	0x7F38 = -20.0 dBm 0x8000 = 0 dBm 0x8037 = 5.5 dBm Each bit represents 0.1 dBm	RO	0

Table 29—10GBASE-T RX Signal Power Channel D Register (Device 1, Register 0x0090)

Bit(s)	Name	Description	R/W	Default
15:0	RX Signal Power Channel D	0x7F38 = -20.0 dBm 0x8000 = 0 dBm 0x8037 = 5.5 dBm Each bit represents 0.1 dBm	RO	0

Table 30—Skew Delay Channel B Register (Device 1, Register 0x0091)

Bit(s)	Name	Description	R/W	Default
15	Reserved	Set to 0	RO	0
14:8	Skew Delay Channel B	0x40 = -80.00ns 0x7F = -1.25ns 0x00 = 0.00ns 0x3F = 78.75ns Each bit represent 1.25ns represented in 2s complement	RO	0
7:0	Reserved	Set to 00000000	RO	00000000

Table 31—Skew Delay Channel C and D Register (Device 1, Register 0x0092)

Bit(s)	Name	Description	R/W	Default
15	Reserved	Set to 0	RO	0
14:8	Skew Delay Channel D	0x40 = -80.00ns 0x7F = -1.25ns 0x00 = 0.00ns 0x3F = 78.75ns Each bit represent 1.25ns represented in 2s complement	RO	0
7	Reserved	Set to 0	RO	0
6:0	Skew Delay Channel C	0x40 = -80.00ns 0x7F = -1.25ns 0x00 = 0.00ns 0x3F = 78.75ns Each bit represent 1.25ns represented in 2s complement	RO	0

Table 32—10GBASE-T Fast Retrain Status and Control Register (Device 1, Register 0x0093)

Bit(s)	Name	Description	R/W	Default
15:11	LP Fast Retrain Count	Counts number of fast retrains requested by link partner Clears on read. Does not rollover.	RO, RC	0
10:6	LD Fast Retrain Count	Counts number of fast retrains requested by local device Clears on read. Does not rollover.	RO, RC	0
5	Reserved	Set to 0	RO	0
4	Fast Retrain Ability	1 = Fast Retrain capability is supported 0 = Fast Retrain capability is not supported	RO	1
3	Fast Retrain Negotiated	1 = Fast was negotiated (LD and LP both advertised fast retrain) 0 = Fast Retrain was not negotiated	RO	0
2:1	Fast Retrain Signal Type	00 = PHY signals IDLE during fast retrain 01 = PHY signals Local Fault during fast retrain 10 = PHY signals Link Interruption during fast retrains 11 = Reserved	R/W	01
0	Fast Retrain Enable	1 = Fast retrain is enabled 0 = Fast retrain is disabled	R/W	0

## PCS Registers

Register address	Register name	Subclause
3.0	PCS control 1 register	45.2.3.1
3.1	PCS status 1 register	45.2.3.2
3.2, 3.3	PCS device identifier	45.2.3.3
3.4	PCS speed ability	45.2.3.4
3.5, 3.6	PCS devices in package	45.2.3.5
3.7	PCS control 2 register	45.2.3.6
3.8	PCS status 2 register	45.2.3.7
3.14, 3.15	PCS package identifier	45.2.3.8
3.20	EEE capability register	45.2.3.9
3.32	BASE-R and 10GBASE-T PCS status 1 register	45.2.3.13
3.33	BASE-R and 10GBASE-T PCS status 2 register	45.2.3.14



Table 33—PCS Control 1 Register (Device 3, Register 0x0000)

Bit(s)	Name	Description	R/W	Default
15	Software Reset	This register will soft reset the copper unit. 1 = Reset 0 = Normal	R/W, SC	0
14	Loopback	Register 3.0000.14 is physically identical to register T22.0.14. 1 = Loopback 0 = Normal	R/W	0
13	Speed Select	1 = Operation at 10Gps and Above	RO	1
12	Reserved	Set to 0	RO	0
11	Low Power	This register will power down the copper unit. 1 = Low Power mode 0 = Normal	R/W	0
10	Clock Stop Enable	This bit has no effect. Write as 0.	RO	0
9:7	Reserved	Set to 000	R/W	000
6	Speed Select	1 = Operation at 10Gps and Above	RO	1
5:2	Speed Select	0000 = Operation at 10Gbs 1000 = 5Gbs 0111 = 2.5Gbs This register is ignored by the PHY. Actual PCS used is determined by auto-negotiations, or PMA mode select.	RO	0000
1:0	Reserved	Set to 00	RO	00

Table 34—PCS Status 1 Register (Device 3, Register 0x0001)

Bit(s)	Name	Description	R/W	Default
15:12	Reserved	Set to 0000	RO	0000
11	Tx LPI Received	1 = Tx LPI was received 0 = No Tx LPI was received	RO, LH	0
10	Rx LPI Received	1 = Rx LPI was received 0 = No Rx LPI was received	RO, LH	0
9	Tx LPI Indication	1 = Tx LPI is being received 0 = No Tx LPI is being received	RO	0
8	Rx LPI Indication	1 = Rx LPI is being received 0 = No Rx LPI is being received	RO	0
7	Fault	1 = Fault condition 0 = No fault condition	RO	1
6	Clock Stop Capable	1 = The MAC may stop the clock during LPI 0 = Clock is not stoppable	RO	0
5:3	Reserved	Set to 0000	RO	0000
2	Link Status	1 = PCS link up 0 = PCS link down	RO, LL	0
1	Low Power Ability	1 = PCS supports low power	RO	1
0	Reserved	Set to 0	RO	0

Table 35—PCS Device Identifier 1 Register (Device 3, Register 0x0002)

Bit(s)	Name	Description	R/W	Default
15:0	Organizationally Unique Identifier Bit 3:18	Set to 0000000000101011	RO	0x28

Table 36—PCS Device Identifier 2 Register (Device 3, Register 0x0003)

Bit(s)	Name	Description	R/W	Default
15:10	Organizationally Unique Identifier Bit 19:24	Set to 000010	RO	000010
9:4	Model Number	Set to 011010	RO	011010
3:0	Revision Number	Rev Number	RO	1011

Table 37—PCS Speed Ability Register (Device 3, Register 0x0004)

Bit(s)	Name	Description	R/W	Default
15:8	Reserved	Set to 0000000000000000	RO	0
7	5G Capable	1 = Capable of operating at 5G	RO	0
6	2.5G Capable	1 = Capable of operating at 2.5G	RO	0
5:1	Reserved	Set to 0000000000000000	RO	0
0	10G Capable	1 = Capable of operating at 10G	RO	1

Table 38—PCS Devices In Package 1 Register (Device 3, Register 0x0005)

Bit(s)	Name	Description	R/W	Default
15:8	Reserved	Set to 00000000	RO	0
7	Auto-Negotiation Present	1 = Auto-Negotiation present in package	RO	1
6	Reserved	Set to 0	RO	0
5	DTE XS Present	1 = DTE XS present in package 0 = DTE XS not present in package	RO	0
4	PHY XS Present	1 = PHY XS present in package 0 = PHY XS not present in package	RO	1
3	PCS Present	1 = PHY XS present in package 0 = PHY XS not present in package	RO	1
2	WIS Present	1 = WIS present in package 0 = WIS not present in package	RO	0
1	PMD/PMA present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO	1
0	Clause 22 registers present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO	0

Table 39—PCS Devices In Package 2 Register (Device 3, Register 0x0006)

Bit(s)	Name	Description	R/W	Default
15	Vendor Specific Device 2 Present	1 = Vendor Specific Device 2 Present 0 = Vendor Specific Device 2 Not Present	RO	1
14	Vendor Specific Device 1 Present	1 = Vendor Specific Device 1 Present 0 = Vendor Specific Device 1 Not Present	RO	1
13:0	Reserved	Set to 0000000000000000	RO	0

Table 40—PCS Control 2 Register (Device 3, Register 0x0007)

Bit(s)	Name	Description	R/W	Default
15:4	Reserved	Set to 000000000000	RO	0
3:0	PCS Type Selection	1 0 1 1= 5GBASE-T PCS type 1 0 1 0= 2.5GBASE-T PCS type 0 0 1 1= 10GBASE-T PCS type This register is ignored by the PHY. Actual PCS used is determined by auto-negotiations, or PMA mode select.	RO	0011

Table 41—PCS Status 2 Register (Device 3, Register 0x0008)

Bit(s)	Name	Description	R/W	Default
15:14	Device Present	10 = Device responding to this address	RO	10
13	5GBASE-T Capable	1= PCS is able to support 5GBASE-T	RO	0
12	2.5GBASE-T Capable	1= PCS is able to support 2.5GBASE-T	RO	0
11	Transmit Fault	1 = Fault on transmit path, 0 = No fault	RO, LH	1
10	Receive Fault	1 = Fault on receive path, 0 = No fault	RO, LH	1
9:4	Reserved	Set to 0000000	RO	0
3	10GBASE-T Capable	1 = PCS is able to support 10GBASE-T PCS types 0 = PCS is not able to support 10GBASE-T PCS types	RO	1
2	10GBASE-W Capable	1 = PCS is able to support 10GBASE-W PCS types 0 = PCS is not able to support 10GBASE-W PCS types	RO	0
1	10GBASE-X Capable	1 = PCS is able to support 10GBASE-X PCS types 0 = PCS is not able to support 10GBASE-X PCS types	RO	0
0	10GBASE-R Capable	1 = PCS is able to support 10GBASE-R PCS types 0 = PCS is not able to support 10GBASE-R PCS types	RO	0



Table 42—PCS Package Identifier 1 Register (Device 3, Register 0x000E)

Bit(s)	Name	Description	R/W	Default
15:0	Organizationally Unique Identifier Bit 3:18	Set to 000000000101011	RO	0x2B

Table 43—PCS Package Identifier 2 Register (Device 3, Register 0x000F)

Bit(s)	Name	Description	R/W	Default
15:10	Organizationally Unique Identifier Bit 19:24	Set to 000010	RO	000010
9:4	Model Number	Same as 3.0003.9:4	RO	011010
3:0	Revision Number	Same as 3.0003.3:0	RO	1011

Table 44—EEE Capability 1 Register (Device 3, Register 0x0014)

Bit(s)	Name	Description	R/W	Default
15:7	Reserved	Set to 00000000	RO	0
6	10GBASE-KR	1 = EEE is supported 0 = EEE is not supported	RO	0
5	10GBASE-KX4	1 = EEE is supported 0 = EEE is not supported	RO	0
4	1000BASE-KX	1 = EEE is supported 0 = EEE is not supported	RO	0
3	10GBASE-T	1 = EEE is supported 0 = EEE is not supported	RO	1
2	1000BASE-	1 = EEE is supported 0 = EEE is not supported	RO	1
1	100BASE-TX	1 = EEE is supported 0 = EEE is not supported	RO	1
0	Reserved	Set to 0	RO	0

Table 45—10GBASE-T PCS Status 1 Register (Device 3, Register 0x0020)

Bit(s)	Name	Description	R/W	Default
15:13	Reserved	Set to 000	RO	000
12	10GBASE-T Receive Link Status	1 = 10GBASE-T PCS receive link up 0 = 10GBASE-T PCS receive link down	RO	0
11:3	Reserved	Set to 000	RO	000

2	PRBS31 pattern testing ability	0 = PCS not able to support PRBS31 pattern testing	RO	0
1	10GBASE-T PCS High Bit Error Rate	1 = High BER reported 0 = High BER not reported	RO	0
0	10GBASE-T PCS Block Lock	1 = Locked to received blocks 0 = Not locked to received blocks	RO	0

Table 46—10GBASE-T PCS Status 2 Register (Device 3, Register 0x0021)

Bit(s)	Name	Description	R/W	Default
15	Latched Block Lock	1 = PCS Has Block Lock 0 = PCS Does Not Have Block Lock	RO, LL	0
14	Latched High Bit Error Rate	1 = PCS Has Reported High BER 0 = PCS Has Not Reported High BER	RO, LH	0
13:8	Bit Error Rate Counter	Bit Error Rate Counter Counter clears on read. Counter will peg at all 1s.	RO, NR	111111
7:0	Errored Blocks Counter	Errored Blocks Counter Counter clears on read. Counter will peg at all 1s.	RO, NR	0

## Ordering Information

Part number	Speed mode	MAC interface	TX Disable function	Link Indicator on RX_LOS Pin	Case Temp
RP-M10GTP	10Gbps	XFI/5GBASE-R/2500BASE-X/SGMII	YES	YES	0~70°C